Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.008”**

**.**

**.018”**

**.018”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .008”**

**Backside Potential: CATHODE**

**Mask Ref: D2**

**APPROVED BY: DK DIE SIZE .018” X .018” DATE: 10/5/21**

**MFG: FAIRCHILD THICKNESS .008” P/N: 1N456**

**DG 10.1.2**

#### Rev B, 7/1